Journal of Applied Electrochemistry **34**: 291–300, 2004.

Integration of thin electroless copper films in copper interconnect metallization

E. WEBB[1,*], C. WITT[2], T. ANDRYUSCHENKO[1] and J. REID[1]
[1]*Novellus Systems, Inc., 11155 SW Leveton Drive, Tualatin, OR 97061, USA*
[2]*International Sematech, 2706 Montopolis Drive, Austin, TX 78741, USA*
*(*author for correspondence, e-mail: eric.webb@novellus.com)*

Received 14 May 2003; accepted in revised form 14 October 2003

Key words: copper, electroless, electroplating, interconnect, seed repair

Abstract

Deposition of a thin electroless copper films on PVD copper seed layers in interconnect metallization was investigated for formation of a composite seed layer. Issues such as film stress, adhesion, electrical reliability, and hydrogen incorporation were addressed to determine feasibility of the process for the fabrication of real device structures. The formation of blisters between the copper films and underlying barrier layer were observed due to hydrogen incorporation and high level of compressive stress as a result of the electroless deposition process. Optimization of the electroless copper bath and process flow were investigated to minimize blister formation and improve fill enhancement effectiveness. Low temperature postelectroless anneal was found to remove incorporated hydrogen but also decreased overall fill effectiveness. Post-CMP electrical reliability of thin PVD/electroless/copper fill process was found to be equivalent to thick PVD/copper fill process. Potential reliability issues with electroless deposition on poorly seeded features were suggested by *via* yield degradation following final anneal.

1. Introduction

Copper electrodeposition upon physical vapour deposited (PVD) copper seed layers is recognized as the preferred method for filling high aspect ratio, 0.13 μm and smaller interconnect features. The selection of copper electrodeposition was based primarily upon the unique bottom-up filling capability of the process which allows void and seam free formation of high aspect ratio interconnect structures [1]. In addition to void-free filling, deposits with low resistivity and good electromigration properties are also obtained. The limits of electrodeposition to provide void-free fill of interconnects can be reached in two ways. First, using PVD films which are thick compared to the feature width generates a very high aspect ratio prior to plating. In this case, the bottom-up fill capability of the bath is insufficient to avoid formation of a void due to pinch-off near the top centre of the feature. Second, thin PVD Cu films can become discontinuous near the base of high aspect ratio features. In this case, voids form in the plated deposit along the feature sidewalls in areas corresponding to the initial lack of seed coverage.

In addition to Cu electrodeposition, electroless deposition of Cu, Co, and Ni and their alloys have been investigated for use in IC interconnect related applications such as diffusion barriers [2–4], interconnect metallization [5–7], and seed layer enhancement [8]. The conformal nature of known electroless deposition process limits its use as a process to completely fill IC features without void formation. Electroless deposition, in conjunction with preactivation and preclean steps which allow initiation of the electroless process on noncatalytic surfaces, has been explored for the possibility of direct plating on barrier layers [9]. The adhesion of the electroless layer to the activated barrier material is poor as a strong chemical bond does not exist across the barrier–electroless Cu interface [10].

Deposition of electroless films, as well as other conformal films such as CVD copper [11], have been recognized to provide a continuous metal seed layer allowing for efficient bottom-up electroplating of copper interconnects. The need for the conformal metal layer increases when the width of features is small and the aspect ratio is large, or when the PVD seed thickness is extremely thin such that electroplating fails to provide void-free feature fill. Future device generations will require thinner PVD seed layers to avoid pinch-off at the feature neck during electroplating. The thinner PVD seed layers reduce the copper coverage near the feature base which results in bottom void formation. One approach to resolving the conflicting requirements of utilizing thinner PVD seed layers to avoid pinch-off and using thicker PVD layers to generate continuous films is

the combination of thin PVD films with thin conformal electroless copper films to form a composite seed layer of low overall thickness and good continuity.

Electroless copper plating is a relatively simple process as there is no requirement for an external power supply or current shaping hardware. Smooth and uniform copper films with relatively low resistivity have been demonstrated [6]. Typical copper electroless baths contain copper sulphate, EDTA as a complexing agent, formaldehyde as a reducing agent, sodium hydroxide, and cyanide containing additives to improve bath stability. However, due to the toxicity and environmental impacts of formaldehyde, glyoxylic acid has been used to replace formaldehyde [12]. The addition of cyanide containing additives is not attractive from a large scale process point of view. Other drawbacks of the electroless process are the incorporation of hydrogen within the deposit as well as the inherent instability of the electroless bath.

The feasibility of integration of an electroless copper process step in a process sequence for copper metallization has been investigated. Process results such as feature fill, uniformity, resistivity, adhesion, and electrical reliability are reported. Integration challenges such as blister formation, postanneal void formation, bath stability, and process control have been addressed. Bath composition and plating conditions have been investigated.

2. Experimental details

The substrates used in this study typically consisted of Si/SiO_2/250–300 Å Ta barrier/100–1000 Å PVD Cu seed film stack on 200 mm wafers. To study fill enhancement, 0.18 μm, 6:1 aspect ratio *vias* with 300 Å PVD Ta followed by 500 Å PVD copper seed were used. The electroless plating solution was composed of $CuSO4 \cdot 5H_2O$, ethylenediamine tetraacetic acid (EDTA), and glyoxylic acid. The pH value was adjusted with the addition of tetramethylammonium hydroxide (TMAH). Various suppressing organic additives were investigated with respect to deposition rate and bath stability. The range of plating temperatures investigated was from 40 to 70 °C.

In formulating the bath composition it was found that the presence of a suppressing polymer such as a low molecular weight polyethylene glycol (PEG) resulted in higher bath stability baths and low plating rates at a high plating temperature. In addition, to reduce the complexing agent concentration and improve bath stability, the concentration of copper metal in the bath was normally held to 1 g l^{-1}, and a 2:1 ratio of EDTA:Cu was found to be sufficient to avoid copper hydroxide precipitation. The relatively low EDTA concentration reduces the amount of TMAH required to achieve the desired operating pH. Table 1 summarizes bath and plating conditions used in this study.

Table 1. Typical electroless copper bath comparison

Bath component	Nominal concentrations
Cu metal	1–2 g l^{-1}
Complexing agent	9–23 g l^{-1}
Reducing agent	5–8 g l^{-1}
Suppressor	10–100 ppm
Operating conditions	
pH (TMAH)	12.0–12.5
Temperature	65 °C
Plating rate	50 Å min^{-1}

Thickness, resistivity and uniformity values were determined by four point probe resistance measurements (RS-75, KLA-Tencor) in combination with MetaPULSE 300 (Rudolph Technologies) measurements. The MetaPULSE 300 uses picosecond ultrasonic laser sonar to measure Cu film thickness. *Via* fill images were analysed with focused ion beam/scanning electron microscopy (FIB/SEM). Thermal annealing was carried out in a forming gas environment. Wafer curvature measurements were carried out on FLX 2320 wafer curvature measurement equipment.

3. Results and discussion

3.1. *Process sequences*

Figure 1 shows possible process sequences for integration of electroless copper deposition process in copper interconnect metallization. The simplest sequence is shown in Figure 1(a), which consists of electroless deposition directly on a freshly seeded wafer to a thickness in the range 100–200 Å. The actual required thickness for complete seed enhancement will depend on the PVD seed thickness, feature width, and feature aspect ratio. Typically for 0.18 μm, 6:1 aspect ratio *vias* seeded with 500 Å PVD copper, about 100–150 Å electroless deposition was required. Bulk copper electrodeposition in a typical acid copper plating bath containing additive follows electroless deposition to

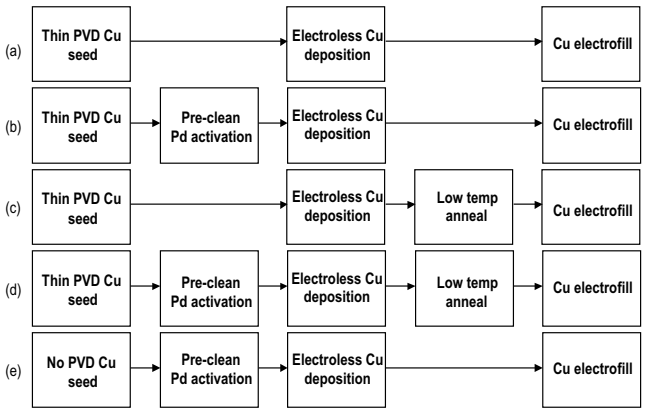

Fig. 1. Possible process sequence for incorporation of electroless copper deposition in for Cu interconnect metallization.

allow for bottom-up fill of interconnect features. Other sequences are shown in Figure 1(b)–(d). Preclean and Pd activation steps are frequently discussed in the literature, see for example [5], and have been found to provide catalytic sites for electroless deposition on noncatalytic surfaces. However, due to the acidic nature of the treatment and the very thin layer of copper seed that exists within the features, as well as the increased process time and process complexity, this process sequence is undesirable. With the use of the pre-activation sequence, plating of copper within the features will take place both on PVD Cu seed and on barrier/barrier oxide material. Direct electroless plating of copper on an activated tantalum oxide surface is known to exhibit serious adhesion problems with sufficient copper overburden. The process sequence shown in Figure 1(c) represents the addition of a low temperature postelectroless anneal step. A low temperature anneal step has been shown to reduce the amount of hydrogen incorporated in the electroless deposit [13, 14] which may be required to minimize the compressive stress exerted on the film stack and reduce the possibility of blister formation. However, the use of a postelectroless anneal step must be weighed against the degradation in fill performance as a result of the anneal.

3.2. *Fill enhancement*

The process sequence shown in Figure 1(a) was used to evaluate the fill enhancement capability of the electroless copper layer. Figure 2 shows fill results on 0.18 μm, 6:1 aspect ratio *vias* seeded with 500 Å PVD copper. Electroless copper films were plated to thicknesses ranging from 75 to 175 Å with bath conditions in the ranges given in Table 1. The plating rate was approximately 50 Å min^{-1} and the rotation rate was 50 rpm for 200 mm wafers. About 24 h following electroless deposition, 0.25 μm copper was electroplated in a commercial acid–copper electroplating bath to provide bottom-up feature fill. The results indicate that for the particular feature studied, 75 Å was insufficient to provide optimal fill enhancement. However, 75 Å electroless deposition reduced the size of the bottom voids compared to the case of no electroless deposition. An electroless thickness of 125 Å and above enabled complete feature fill during electroplating.

The effect of the delay in transfer between the electroless deposition step and the electroplating step was investigated. Following electroless Cu, samples underwent Cu electroplating with three different delay conditions between electroless Cu and electroplated Cu: (i) immediate transfer between electroless Cu and electroplating; (ii) samples stored after electroless Cu deposition for 24 h prior to electroplating; and (iii) samples stored after electroless Cu deposition for one week prior to electroplating. Four electroless thickness values were tested: 75, 125, 175 and 225 Å. Electroless Cu thickness of 75 Å was insufficient to fully eliminate bottom voids but 125, 175 and 225 Å electroless

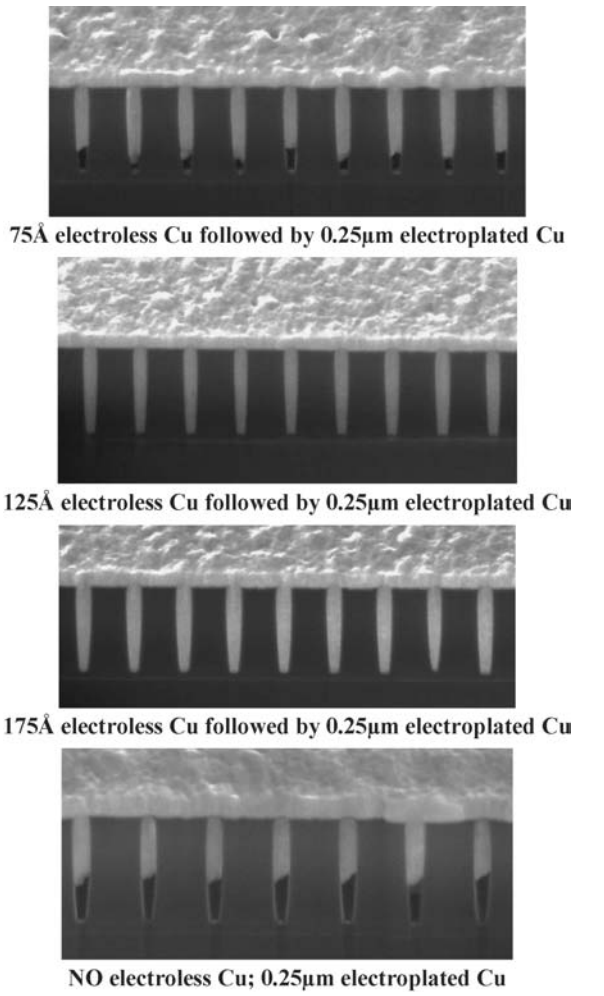

Fig. 2. FIB/SEM images of feature fill of 0.18 μm × 1.1 μm, 6:1 aspect ratio *vias* with 300 Å PVD Ta barrier and 500 Å PVD Cu seed. Electroless Cu was deposited on the PVD Cu seed to thickness values of 0, 75, 125, 175 Å followed by electroplating of 0.25 μm of copper.

thicknesses allowed complete fill for both immediate transfer and 24 h delay conditions. Figure 3 shows fill results following 125, 175 and 225 Å electroless Cu deposition and 0.25 μm electroplating for two delay conditions: immediate transfer and one week delay between electroless Cu and electroplating. After one week delay between electroless and electroplating the fill results were variable. The full fill result after one week delay using 125 Å electroless thickness suggests good resistance of the electroless film to damage by oxidation or agglomeration at room temperature, however as noted by the 175 Å case one week delay represents conditions where fill may become marginal.

The effect of the electroless copper layer on the seed condition is important to predict impact on subsequent fill characteristics of the structure. Figure 4 shows SEM results with and without 125 Å electroless copper deposition on substrates with 300 Å PVD Ta and 500 Å PVD copper seed thickness on the field. The results in Figure 4(a) and (b) show that the copper coverage within the feature with PVD alone is very sparse, and at the bottom sidewalls very little copper

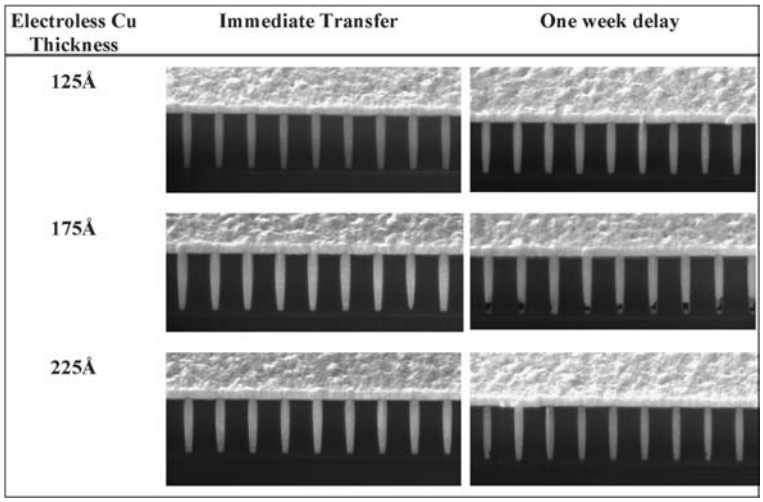

Fig. 3. FIB/SEM images of 0.18 μm × 1.1 μm, 6:1 aspect ratio *vias* with 300 Å PVD Ta barrier and 500 Å PVD Cu seed for two delay sequences: immediate transfer to electroplating bath following electroless Cu deposition and one week delay between electroless Cu plating and electrofill. Electroless Cu was deposited on the PVD Cu seed to thickness values of 125 and 175 Å.

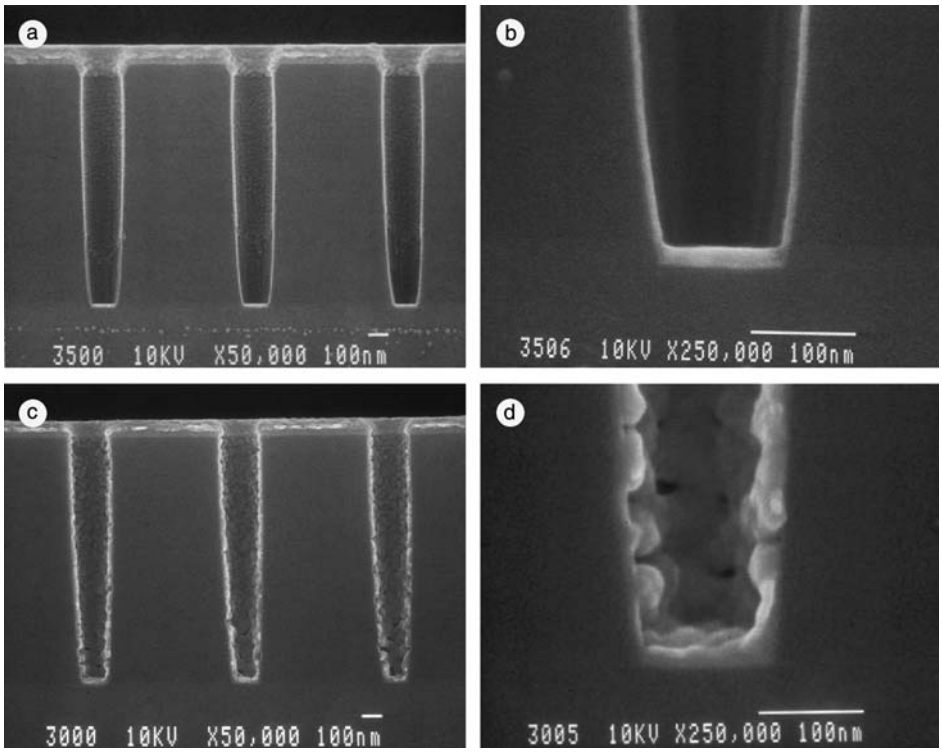

Fig. 4. SEM images of conformal coverage of copper electroless film, (a) and (b) are SEM images of 500 Å PVD seed only, (c) and (d) are SEM images of 500 Å PVD seed with the addition of 125 Å electroless copper.

exists. Thus, the large bottom voids shown in the fill results shown in Figure 2 without electroless deposition are not surprising. Figure 4(c) and (d) show the copper coverage after deposition of a conformal electroless copper layer. Significant improvement in the copper coverage is seen along the entire length of the *vias*. Since no Pd preactivation of the wafers was used prior to electroless plating, some copper islands or oxidized copper must have been present prior to electroless plating and served as initiation sites for the electroless process. However the lack of copper nucleation sites leads to an agglomerated deposit appearance as noted near the bottom of the *vias*.

The effects of process variable changes during electroless Cu deposition on the overall fill effectiveness was investigated, in particular the effects of rotation rate, additives, and complexing agent were investigated. Several interesting observations were noted. First, both an increase in the rotation rate and the addition of a stabilizer molecule resulted in a decrease in the overall

fill effectiveness of the process sequence shown in Figure 1(a). Qualitative arguments based on these observations can be made that suggest an intermediate cuprous species may play a key role in the electroless Cu deposition process. An intermediate cuprous species participating in the electroless reaction has been suggested previously [2]. An increase in the rotation rate would result in an increased rate of transport of the intermediate species away from the feature and subsequently a reduced rate of deposition within the feature. A similar argument can be made to support the observation that excess stabilizer additive decreased the fill effectiveness. In this context, we refer to a stabilizer additive to be one which forms a strong complex with cuprous ions [15–18]. The addition of the stabilizer additive would drastically decrease the plating rate through complexation with cuprous ions. Cuprous ion complexation slows the rate of electron transfer from cuprous to copper metal and stabilizes the cuprous ion state, which would enhance the ability of cuprous ions to be transported away from the feature base. A second interesting observation is the effect of the EDTA additive concentration. Increasing the EDTA concentration was found to decrease the overall fill effectiveness, an effect which may be explained by the strong etching ability of the EDTA molecule on the copper substrate. When the EDTA concentration is too large and the seed thickness near the feature base is extremely thin, the thin seed will be etched away during the induction period prior to the initiation of plating, resulting in degraded electroless copper coverage at the base of the features.

3.3. *Uniformity*

The uniformity of the electroless process across 200 and 300 mm wafers was evaluated. The within wafer uniformity has been found to be consistently less than 2.5% one sigma for electroless bath containing a suppressor additive. The excellent across wafer uniformity is not surprising given the conformal nature of the electroless process, uniform mass transfer characteristics of the plating cell, and the lack of primary current distributions inherent in electroless processes. Uniformity below 5% one sigma was achieved for electroless thicknesses as low as 100 Å.

3.4. *Resistivity*

The resistivity of the electroless copper layer was evaluated. The Cu film thickness was determined through Metapulse measurement and the resistance was evaluated with four point probe resistance measurements. In order to accurately measure the thickness, 1000 Å electroless layers were deposited and annealed at 250 °C for 90 s. The resistivity of these films was found to be 1.9 ± 0.1 $\mu\Omega$ cm. This value is consistent with values reported elsewhere [2], and although it is known that the resistivity increases with decreasing thickness, the result indicates that the electroless layer would not have significant impact on the overall resistivity of the copper metal film stack.

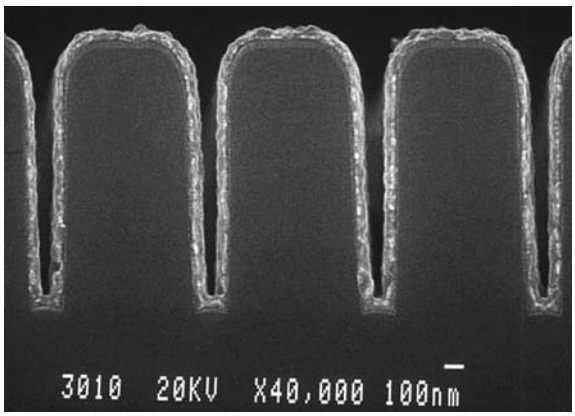

Fig. 5. SEM image of the deposition of 70 Å of electrodes on a Ta substrate following Pd activation.

3.5. *Adhesion*

3.5.1. *Plating on $Si/SiO_2/Ta$*

The adhesion of electroless copper films deposited directly on Ta barrier was evaluated. The Ta substrates were first activated for 120 s at 60 °C in a commercial Pd activation solution. The substrates were then electrolessly plated with copper at 65 °C for 2 min. Figure 5 shows SEM images of approximately 70 Å of electroless Cu plated on Pd activated Ta substrate. The conformal nature of the deposition process is clearly evident. Following deposition of a 1 μm electroplated Cu film, adhesion failure occurred at the Ta/Cu interface showing the lack of strong bonding at this interface. Similar adhesion results were noted on all other commonly available barrier materials. This process sequence would not be acceptable in the current metallization sequence as failure would occur during CMP.

3.5.2. *Plating on $Si/SiO_2/Ta/PVD\ Cu_{seed}$*

Considering the poor adhesion of the electroless copper film to the Ta barrier, the adhesion of electrolessly deposited copper on $Si/SiO_2/Ta$ substrates seeded with thin layers of 100 Å PVD copper was evaluated. Table 2 indicates adhesion strength, G_c in J m^{-2}, from a four point bend test on the $Si/SiO_2/Ta/PVD\ Cu_{seed}$/film stack following the deposition of 1 μm electroplated copper (control) and 120 Å electroless copper and 1 μm

Table 2. Adhesion test for $Si/SiO_2/Ta/PVD\ Cu_{seed}$/plated Cu with and without 120 Å electroless Cu following the process sequence given in Figure 1(a)

Sample	G_c /(J m^{-2})	Std. dev.	Number of samples
Control	11.5	7.8	3
With electroless Cu	18.3	8.9	4

electroplated copper. No degradation in the adhesion was noted with the addition of the electroless Cu film and no failures at any Cu interface was noted. Failure in all cases was found at the SiO_2/Ta interface which indicates that the weakest interface of the film stack is the Ta barrier on the SiO_2 dielectric.

3.6. *Electrical reliability*

Via chain yields and other electrical properties were obtained using dual damascene structures formed using SiO_2 as interlayer dielectric and SiN as an etch stop layer. Total thickness of the dual damascene layer was 1.5 μm including $\sim$0.4 μm line thickness and $\sim$1.1 μm *via* level thickness. After etch and clean, all wafers received 250 Å PVD Ta and PVD seed with thicknesses of 100, 300 and 1000 Å. Excess copper removal after electroplating was achieved by chemical mechanical polishing (CMP). A standard metallization process not expected to contribute to *via* chain yield loss was used to fabricate the metal layer used to connect damascene *via* chain structures. Electrical measurements were performed after CMP of the damascene layer, after final SiO_2/SiN passivation, and after bond pad opening and Al bond pad metallization.

To show the effect of electroless Cu deposition on the electrical performance of copper lines, the resistance of 0.25 μm wide serpentine patterns were measured. The resistance distributions for a 1000 Å PVD seed and 100 Å PVD with 120 Å electroless copper are shown in Figure 6. The sample group using the 100 Å seed and no electroless showed an increased median resistance and a wider distribution as compared to the other samples. This could be indicative of voiding in the serpentine trenches during copper electrofill even though it is well known that voiding in trenches is relatively insensitive to seed coverage compared to the behaviour in *vias*.

Figure 7 shows post-CMP *via* chain yield results for several initial PVD seed thicknesses and following

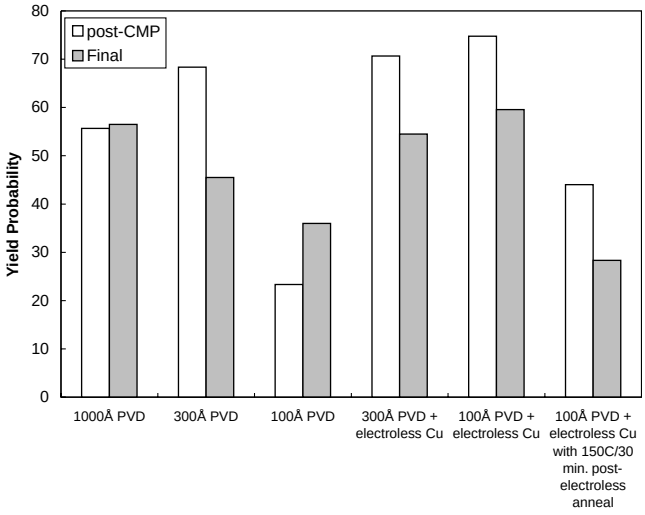

Fig. 7. *Via* chain yield of 0.25 μm wide lines for PVD–electroless Cu process conditions.

electroless deposition on 100 and 300 Å PVD seed. The result indicates that reducing the copper seed thickness from 1000 to 100 Å reduces the yield from 55% to less than 25%. The addition of electroless deposition on the 100 Å PVD samples resulted in yield increases from 25% to values between 65 and 75% depending on electroless additive and deposition temperature. This yield is comparable or higher than the reference process using 1000 Å PVD seed only (55%). The effect of a postelectroless/preplate anneal was investigated as a method to reduce the formation of blisters, as discussed below, and is also shown in Figure 7. The anneal step resulted in a degradation of the *via* chain yield from 65 to 75% to less than 50%. The degradation was possibly due to copper oxidation and/or agglomeration during the long-time low-temperature anneal conditions.

Figure 7 also shows the *via* chain yield results following final processing which included a 380 °C/

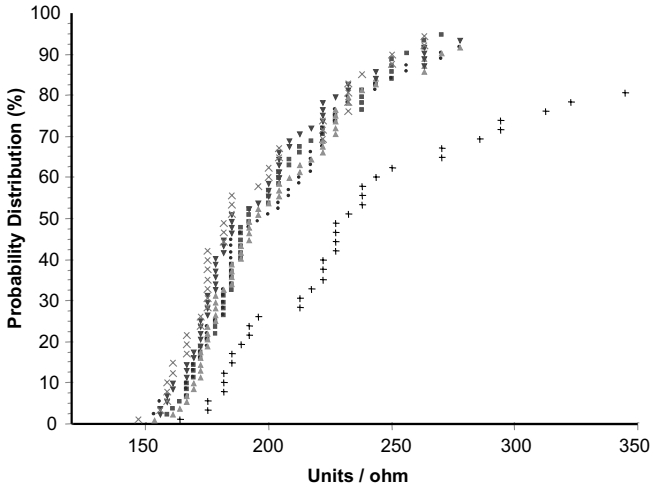

Fig. 6. Serpentine line resistance of 0.25 μm wide trenches for the three PVD–electroless conditions: 1000 Å PVD Cu-no electroless Cu (×); 100 Å PVD Cu-no electroless Cu (+); and 100 Å PVD Cu-120 Å electroless Cu (▲, ▼, ●, ■).

30 min anneal. In most cases, a larger yield loss following final processing was seen with electroless Cu deposition. The increased yield drop was most likely due to poor adhesion between the electroless Cu layer and poorly seeded sidewall regions, which represents a risk for integration of the electroless process. The electroless films did provide improvement of *via* chain yield after final processing compared to structures seeded with 100 Å PVD layers alone, however, this 100 Å PVD film is clearly inadequate for these structures. The yield drop following final processing requires further investigation to determine the impact on real device fabrication.

3.7. *Blistering*

The formation of blisters during or after electroless copper deposition is a widely observed occurrence. The formation of blisters has been reported to be due to the incorporation and accumulation of hydrogen gas at weak Cu/substrate interfaces. The addition of additives such as potassium ferrocyanide and 2-2′ dipyridyl [15] have been reported to improve the ductility of the copper films by reducing the amount of incorporated hydrogen, which in turn reduced the formation of hydrogen containing voids. In addition, the application of a mild temperature anneal for an extended period of time was found to remove molecular hydrogen within the deposit [14]. Recently, Hsu et al. [10] reported results on the deposition of electroless copper layers on Si/SiO_2/barrier/Cu_{seed} substrate where the barrier layer was either TiN, Ta, or TaN. They observed blister formation at the copper/barrier interface even with the addition of potassium ferrocyanide and 2-2′ dipyridyl. Blister formation was attributed to hydrogen evolution, incorporation, and accumulation within the electroless layer.

Electroless copper films were deposited on $Si/SiO_2/Ta$ substrates seeded with PVD copper of thicknesses ranging from 100 to 1200 Å. Thin electroless copper films were deposited followed by the deposition of electroplated copper. Both patterned and blanket wafers were investigated. Figure 8 shows a blister about 30 μm in diameter which formed after electroless and electroplated copper layers were deposited on a patterned wafer. Blisters were found to form most frequently in large (>5 μm) recessed regions on patterned wafers. Similar blisters were observed on blanket wafers, and the number of blisters was found to be critically dependent on the thickness of each metal layer. Thinner copper seed layers led to more blisters for a given electroless thickness, while the deposition of thicker electroless layer led to increased blisters for a given seed thickness. Figure 9 shows a plot of the PVD Cu seed thickness vs the electroless Cu thickness for the observation of blisters. The solid line represents the thinnest electroless film thickness for a given PVD Cu seed thickness where blisters were observed. The dotted line represents the thickest electroless film thickness for a given PVD Cu seed thickness where blisters were not observed. Analysis of the failure showed that the blisters

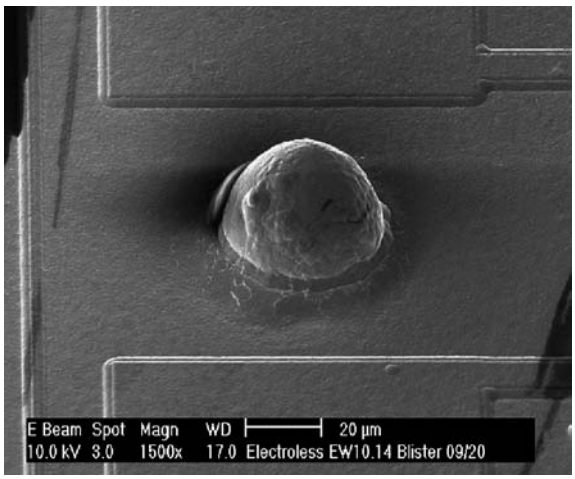

Fig. 8. SEM image of a blister which formed on the wafer after deposition of electroless copper and electroplated copper.

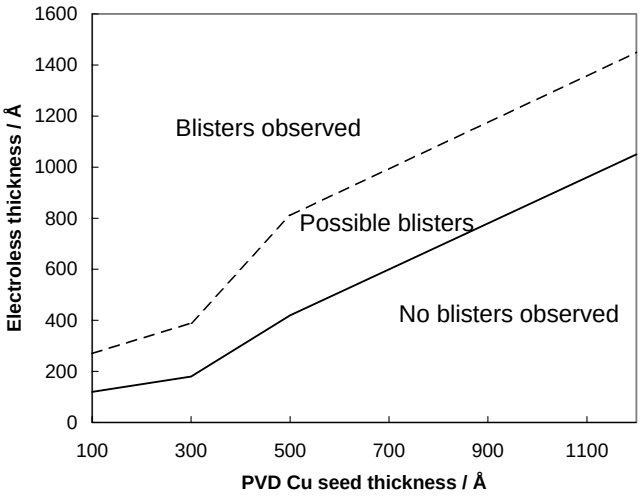

Fig. 9. Plot of the conditions for blister formation as a function of PVD Cu seed thickness and electroless Cu thickness. The lower solid line represents the thinnest electroless layer for a given PVD Cu seed thickness where blisters were observed. The upper dotted line represents the thickest electroless layer for a given PVD Cu seed thickness where blisters were not observed.

formed at the Ta/SiO_2 interface, not at the Cu/barrier interface. The observation of Ta/SiO_2 failure is consistent with the adhesion results presented above which showed the Ta/SiO_2 interface to be the weakest. The mechanism of failure may be due to the high compressive stress of the electroless layer or due to chemical attack of the barrier by incorporated hydrogen. The stress of the electroless layers were analysed by wafer curvature measurements and found to be on the order of 2 GPa compressive for a 200 Å thick electroless film. The highly compressive film could lead to local failure at defects at the Ta/SiO_2 interface. Further, deposition of the tensile electroplated copper film facilitates the local failure and subsequent blister formation.

To determine the presence of hydrogen within the electroless deposits, out-gassing species were detected by

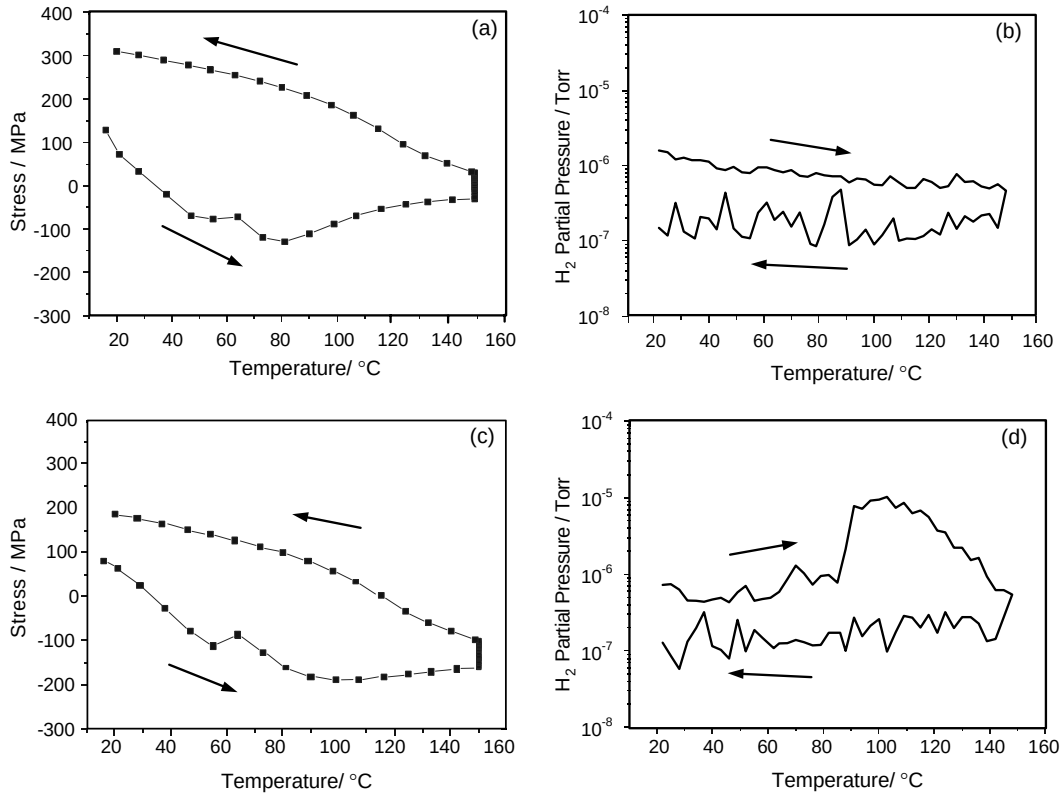

Fig. 10. Stress and hydrogen partial pressure measurements in the copper film during temperature cycling, (a) and (b) Stress and hydrogen partial pressure, respectively, for 1.0 μm electroplated copper film on 100 Å PVD copper seed. (c) and (d) Stress and hydrogen partial pressure, respectively, 1 μm electroplated copper on 120 Å electroless Cu and 100 Å PVD copper seed.

residual gas analysis (RGA) in the vacuum chamber, as a function of temperature. Simultaneously, the wafer curvature was used to determine the film stress. Wafer curvature reference measurements were made after barrier PVD seed deposition. The contribution of the 100 Å PVD seed film to curvature is assumed to be small; hence, the measured stress data represent the actual stress in the entire copper film on top of the barrier. Stress and hydrogen partial pressure data were recorded during the entire temperature cycle of heating from room temperature to 150 °C, holding 150 °C for 30 min, and cooling.

Figure 10(a) and (b) shows stress and hydrogen partial pressure, respectively, of a wafer that had a 100 Å PVD seed layer and 1 μm electroplated copper. Upon heating, the film shows compressive stresses as expected from the difference in thermal expansion between copper and the silicon substrate. The yield stress is about −230 MPa. The small decrease in compressive stress between 60 and 70 °C is believed to be attributed to initial recrystallization of the electroplated copper. While holding at 150 °C the compressive stress is relaxed to about −80 MPa; this is thought to be due to diffusional or plastic creep. Upon cooling, the stress undergoes a transition to tensile. The hydrogen content in the residual gas was monitored between 1×10^{-7} and 1×10^{-6} torr during the entire cycle.

The previously described measurement was repeated on a sample that had 120 Å electroless copper deposited prior to electroplated copper. The results are shown in Figure 10(c) and (d) for stress and hydrogen partial pressure, respectively. Compared to the reference sample (Figure 10(a) and (b)), this film stack exhibited significant hydrogen desorption. During heating the hydrogen partial pressure reached about 1×10^{-5} torr. After holding at 150 °C for 30 min, a low hydrogen level of 1×10^{-7} torr was reached. This suggests that most of the hydrogen enclosed in the copper had diffused out. Interestingly, the compressive yield stress of this copper film decreased to about −120 MPa. To verify whether the hydrogen originates from the electroless copper, a third sample was prepared as previously described, with the addition of a postelectroless anneal of 150 °C for 30 min. The stress behaviour and amount of desorbed hydrogen decreased to an amount comparable to the reference sample in Figure 10(a) and (b). Furthermore, the compressive yield stress of this sample was about −200 MPa. This result suggests that the hydrogen content and the yield stress of the copper film are correlated. From a processing perspective, the data can be used to determine the optimal heat treatment after electroless deposition. However, annealing was found to have a detrimental effect on the fill properties of small features as illustrated in Figure 11. The FIB/SEM images show that as postelectroless anneal temperature increases, seed related voids become more frequent and larger due to copper seed agglomeration and oxidation.

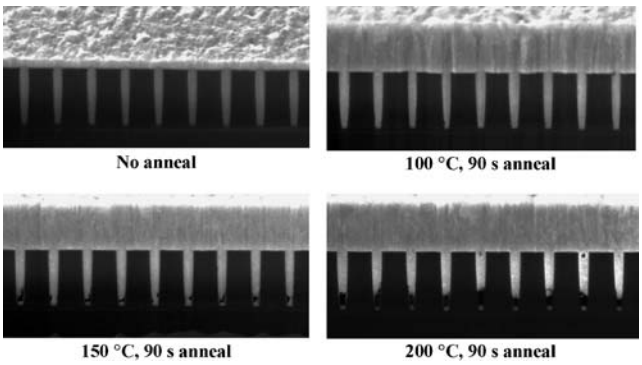

Fig. 11. SEM/FIB images of the effect of postelectroless anneal temperatures on feature fill of 0.18 μm × 1.1 μm, 6:1 aspect ratio *vias* with 300 Å PVD Ta barrier and 500 Å PVD Cu seed and 120 Å electroless Cu.

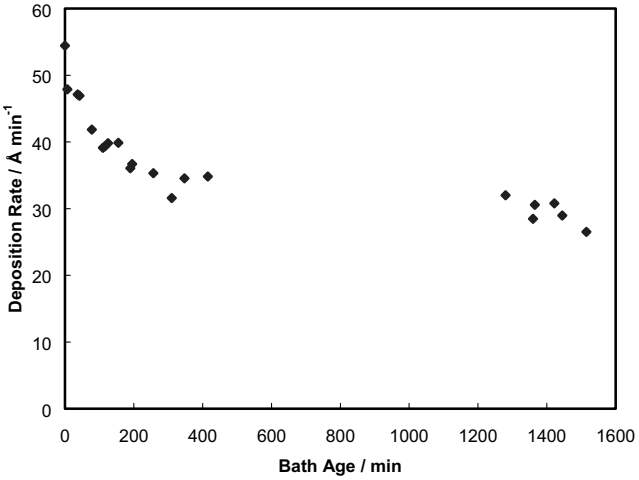

Fig. 12. Electroless deposition rate as a function of bath age for a 24 h bath age test.

To reduce the occurrence of blisters, modifications to the chemistry and process conditions were made. It was found that the number of blisters was directly related to the deposition rate, a slower rate of deposition led to fewer blisters. In addition, it was found that increasing the plating temperature led to the formation of fewer blisters. Both process modifications are consistent with the importance of removal of hydrogen gas prior to its incorporation. A slower rate of deposition allows desorption of hydrogen to occur prior to incorporation. Similarly, a higher plating temperature allows for an increased rate of hydrogen desorption. To maximize the plating temperature while minimizing the plating rate, a strongly suppressing polymer molecule was used. The addition of 10–100 ppm PEG (average molecular weight 600) allows for plating of approximately 50 Å min^{-1} at 65 °C.

3.8. *Bath stability and control*

Experiments were performed to investigate the stability of the electroless bath and the ability to control and maintain important process metrics such as within wafer uniformity, electroless thickness, and fill performance with use of the process sequence shown in Figure 1(a). The bath was maintained and replenished with a 25% bleed and feed per day as shown by the arrows on the graph. In this test the plating rate was allowed to drift downward between fresh bath doses as the side reaction between reducing agent and hydroxide ion took place. During the bath age test no spontaneous electroless copper plate-out on plating cell surfaces was observed. Within wafer uniformity was monitored, and other than the two initial wafer measurements, the within wafer uniformity is less than 2% one sigma for blanket wafers deposited with 150 Å electroless Cu.

Figure 12 shows the deposition rate as a function of time over a 24 h test period; a decrease in rate over the time period of the test due primarily to the side reaction of the reducing agent with hydroxide ions. To control accurately the thickness of the copper film based on time of deposition, precise control of pH, reducing agent, temperature, and other parameters is necessary but very difficult. More accurate control of the actual deposit thickness can be obtained by controlling deposition time based on the amount of copper deposited while allowing process rate to vary slightly based on available bath control technology.

One method to control the overall electroless thickness is to use a full wafer four point probe resistance measurement method [19]. Figure 13 shows the full wafer resistance measurement of a 1200 Å Cu seed wafer which underwent electroless Cu deposition. When the wafer enters the bath the resistance increases. Initially the wafer resistance remains constant during the induction period, and then as plating commences, the wafer resistance decreases. When the wafer resistance reaches the target resistance (thickness) the processing is stopped by removing the wafer from the bath. Using this method deposition thickness is accurately controlled by variation of deposition time.

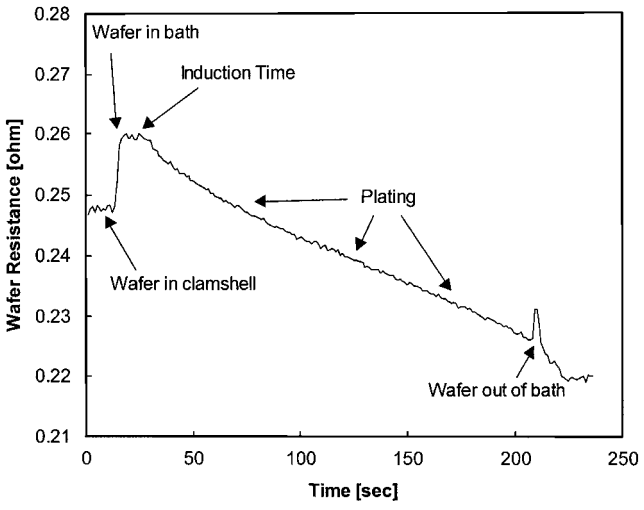

Fig. 13. Full wafer resistance measurement.

4. Conclusions

The feasibility of electroless copper deposition in copper metallization schemes was evaluated. Integration of electroless plating processes as part of a copper interconnect metallization scheme has been accomplished using a simple process sequence of thin PVD Cu seed followed by direct electroless plating and feature fill with electroplated copper. The application of a thin electroless layer was found to significantly enhance the fill capability of current commercial acid copper electroplating baths on small, high aspect ratio features with thin PVD copper seed layers. Electrical reliability of the thin PVD/electroless/electroplated copper layers was equivalent to thick PVD/electroplated copper layer controls following CMP. The significance of *via* chain yield loss on features with electroless films following thermal cycling requires further investigation. Blisters associated with barrier/dielectric adhesion loss on electroless copper treated substrate represent an integration issue which is not fully resolved. The amount of hydrogen incorporated within the deposit and subsequent blister formation can be reduced through changes in process variables. However, since hydrogen gas is produced as part of the oxidation of glyoxylic acid on copper, elimination of all hydrogen cannot be achieved without significant modification to the bath chemistry. During electroless deposition, the target electroless thickness was controlled with the use of an in-line cross wafer resistance measurement method. The in-line method does not rely on precise control of the deposition rate, which can decrease as the bath ages due to the side reaction of the reducing agent with hydroxide ions. Bath age experiments with bleed and feed have demonstrated the ability to maintain a stable bath capable of consistent within wafer uniformity.

References

1. J. Reid, S. Mayer, E. Broadbent, E. Klawuhn and K. Ashtiani, *Solid State Technol.* **43** (2000) 86.
2. S. Lopatin, Y. Shacham-Diamand, V. Dubin and P.K. Vasudev, *SPIE* **3214** (1997) 21.
3. S. Lopatin, Y. Shacham-Diamand, V. Dubin, P.K. Vasudev, J. Pellerin and B. Zhao, *Mater. Res. Soc. Symp. Proc.* **451** (1997) 463.
4. E.J. O'Sullivan, A.G. Schrott, M. Paunovic, C.J. Sambucetti, J.R. Marino, P.J. Bailey, S. Kaja and K.W. Semkow, *IBM J. Res. Develop.* **42** (1998) 607.
5. C.H. Ting, M. Paunovic, P.L. Pai and G. Chiu, *J. Electrochem. Soc.* **136** (1989) 462.
6. V. Dubin, Y. Shacham-Diamand, B. Zhao, P.K. Vasudev and C.H. Ting, *J. Electrochem. Soc.* **144** (1997) 898.
7. M. Desilva, Y. Shacham-Diamand, R. Soave and H. Kim, *J. Electrochem. Soc.* **143** (1996) L78.
8. T. Andryuschenko and J. Reid, *Proc. IITC Conf.* (2000) 33.
9. H. Hsu, C. Hsieh, M. Chen, S. Lin and J. Yeh, *J. Electrochem. Soc.* **148** (2001) C590.
10. H. Hsu, K. Lin, S. Lin and J. Yeh, *J. Electrochem. Soc.* **148** (2001) C47.
11. K. Shim, H. Lee, O. Kwon, H. Park, W. Koh and S. Kang, *J. Electrochem. Soc.* **149** (2002) G109.
12. H. Honma and T. Kobayashi, *J. Electrochem. Soc.* **141** (1994) 730.
13. Y. Okinaka and S. Nakahara, *J. Electrochem. Soc.* **123** (1976) 475.
14. S. Nakahara, Y. Okinaka and H.K. Straschil, *J. Electrochem. Soc.* **136** (1989) 1120.
15. Y. Okinaka and H.K. Straschil, *J. Electrochem. Soc.* **133** (1986) 2608.
16. A. Hung, *J. Electrochem. Soc.* **132** (1985) 1047.
17. K. Kondo, K. Kojima, N. Ishida and M. Irie, *J. Electrochem. Soc.* **140** (1993) 1598.
18. J. Shu, B.P.A. Grandjean and S. Kaliaguine, *Ind. Eng. Chem. Res.* **36** (1997) 1632.
19. J. Reid, et al., Patent pending.